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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/672,803	09/28/2000	Jiren Yuan	026125-068	8153

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EXAMINER	
TON, MY TRANG	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/672,803	YUAN, JIREN	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE filed on 01/14/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-53 and 58-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *38-49 and 61-65* is/are allowed.

6)☒ Claim(s) *32-34,36,37,58,60* is/are rejected.

7)☒ Claim(s) *35,50-53, 59* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 32-34, 36, 37, 58 and 60 are rejected under 35 U.S.C. 102(b) as being anticipated by Carley et al (the prior art submitted in PTOL 1449).

The prior art discloses in Fig. 1 a sample-and-hold architecture including:

a control signal generator (not show, providing clock signal $\phi 1$, $\phi 2$ to control switches S & R) for controlling an analog input signal (Iin) to the charge sampling circuit (Fig. 1) ; and

an integrator (capacitor, R) for integrating directly the analog input signal (Iin) during a sampling phase (when ON) responsive to a sampling signal ($\phi 1$, $\phi 2$) from the control signal generator (not show), wherein a current of the analog input signal (Iin) is integrated to an integrated charge for producing one of a proportional voltage sample and a proportional current sample at a signal output upon completion of the sampling phase (during charging phase) as recited in claim 32.

Element S reads on a sampling switch having a signal input for analog input signals (Iin), a signal output connected to a signal input of the integrator (capacitor, R), and a control input connected to a sampling signal ($\phi 1$, $\phi 2$) output of the control signal generator (not show) for controlling the switch (S) to be on only when the sampling

signal from the generator is in a sampling phase (during charging) as recited in claim 33.

The control signal generator (not show) controls the integrator (capacitor, R) to hold the sample (when OFF) until a resetting signal from the generator (not show) is applied to a control input of the integrator (ϕ1, ϕ2 apply to R) as recited in claim 34.

The fully-differential circuit discloses in Fig. 1 of the prior art reads on claim 36:

a first charge sampling circuit (circuit connected to Vin+) having a first integrator (capacitor, R connected to Vo+);

a second charge sampling circuit (circuit connected to Vin-) having a second integrator (capacitor, R connected to Vo-);

a first analog input (IB + Iin+) being a signal input of the first charge sampling circuit (circuit connected to Vi+);

a second analog input (IB+Iin-) being a signal input of the second charge sampling circuit (circuit connected to Vi-);

a first signal output (connected to S) being a signal output of the first charge sampling circuit (circuit connected to Vin+);

a second signal output (connected to S) being a signal output of the second charge sampling circuit (circuit connected to Vin-); and

a common control signal generator (not show, providing ϕ1, ϕ2 to control S & R) for controlling an analog input signal provided to the first and second analog inputs (IB+Iin+, IB+Iin-), wherein the first and second integrators (capacitors, R) integrate a respective portion of the analog input signal during a sampling phase (turn ON)

responsive to a sampling signal (ϕ1, ϕ2) from the common control signal generator (not show).

The first integrator (circuit connected to Vi+) and the second integrator (circuit connected to Vin-) form a single differential integrator (FULLY-DIFFERENTIAL) having two inputs (IB+Iin+, IB+Iin-) for integrating a differential current of the analog signal and for producing differential samples at the first signal output and at the second signal output (connected to S) of the differential charge sampling circuit as recited in claim 37.

The method recited in claims 58 and 60 are similarly rejected as claim 32.

Allowable Subject Matter

Claims 35, 50-53, 59 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 38-49 and 61-65 are allowable over the prior art of record.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 12, 2004

MY-TRANG NU TON
PRIMARY EXAMINER